ABSTRACT

A sigma delta interpolator for use in a fractional N synthesizer having a multi-modulus divider for controlling the output frequency of the synthesizer. The sigma delta interpolator includes an accumulator operative for receiving an input signal representing the desired frequency output of the fractional N synthesizer and for generating a digital output signal having M bits, which include N most significant bits and n least significant bits. The N most significant bits output by the accumulator are coupled to the multi-modulus divider and are operative for controlling the operation of the multi-modulus divider. The sigma delta interpolator further includes a delay circuit coupled to the accumulator, which functions to receive the n least significant bits and implement a delay function defined by equation: $1-(1-Z^{-1})^N$, where N corresponds to the order of the sigma delta interpolator.